-- Figures 5A and 5B are a schematic diagram of a third circuit according to the invention; --

Please replace the paragraph beginning on page 3, line 17 with the following re-written paragraph:

-- Figures 6A and 6B are a schematic diagram of a fourth circuit according to the invention; and –

Please replace the paragraph beginning on page 6, line 11 with the following re-written paragraph:

-- Presented below are four embodiments of a cable length measurement apparatus. Embodiment 1 is described below with reference to a block diagram (Figures 2A-2B) and a circuit schematic (Figures 3A-3C). Embodiments 2-4 are described below with reference to circuit diagrams (Figures 4A-6C). A cable length measurement method is described below with reference to a flow chart (Figure 7). Finally, a suitable for use with the cable length measurement invention, is described in greater detail. --

Please replace the heading on page 8, line 10 with the following re-written heading:

-- Overview of Circuit Components (Figures 3A-3C) --

Please replace the paragraph beginning on page 8, line 11 with the following re-written paragraph:

-- F1 & F3 Generator: A programmable interrupt controller (PIC) microcontroller is programmed to produce two frequencies, which can be called F1 and F3. F1 is passed along directly as Fa, in this case, correlating to Figures 2A and 2B. F3, however, is produced by dividing F1 down by a factor, N2 where N2 is an integer. This new frequency, F3, enters into the PLL circuit which is wired as a frequency multiplier. Frequency F1 is derived from the 20MHz input clock by dividing it by a relatively large number and multiplying that by a smaller number, resulting in F1 = x1/x2 * 20Mhz. --

Please replace the paragraph beginning on page 8, line 18 with the following re-written paragraph:

-- PLL Frequency Multiplier & Divide by N1: The PLL is used to "multiply-up" the incoming F3 frequency by the value "N1" to produce F2, called Fb in Figures 2A and 2B. The result is that F2 is exactly equal to F3 * N1 in the average, but includes a factor of error

on a cycle-by-cycle basis, called "jitter." Both characteristics of F2, namely exact average and jitter, are key factors in achieving accurate measurement results. --

Please replace the paragraph beginning on page 8, line 23 with the following re-written paragraph:

-- Sample-Hold Latch (Mixer): This device is key to the theory of operation of this circuit, and is a unique application for a Flip-Flop. This device is referred to in Figures 2A and 2B, but may be better explained as a signal mixer, rather than as a "Sample-Hold Latch." It may also be explained as a pulse-width multiplier. The Flip-Flop is receiving two signals very close in frequency (separated in frequency by only a few Hertz – a tiny percentage) but very different in pulse width. The signal with the narrower pulse width is entering into the "D" input and the signal with 50 percent duty cycle is entering into the "CLK" input. The result at the output "Q" is a frequency equal to the "beat frequency" or frequency difference between the two incoming signals – this is similar to the effect a mixer would have. The output pulse width, however, is the product of the smaller pulse width multiplied up by the factor of the longer incoming cycle time divided by the differences in periods between the two incoming signals. For this reason, the Flip-Flop has the effect of multiplying the incoming pulse width up in width, to a more readable duration, where a high-speed counter would not be necessary. --

Please replace the paragraph beginning on page 9, line 12 with the following re-written paragraph:

-- Figures 2A and 2B are a block diagram of a system for measuring a cable length, according to Embodiment 1 of the cable length measurement invention. The system is composed of two major sections, the cable-length-controlled pulse width oscillator section and the pulse width testing and data output section, as shown in Figures 2A and 2B. Figures 3A-3C are a schematic diagram of a corresponding circuit. --

Please replace the paragraph beginning on page 13, line 8 with the following re-written paragraph:

-- Figures 4A-4C are schematic diagram of a second circuit (Embodiment 2) according to the invention. This circuit and the general operation of this circuit are very similar to Embodiment 1 with the exception that the performance has been improved for shorter cable lengths. With shorter cable lengths applied using the Embodiment 1 circuit, C14 never obtains a charge heavy enough to result in a pulse suitable to clear the U7B flip-

flop. That is, when the output of U10 is low for the great majority of the cycle time (short cables), and when it goes high only briefly and then low again, the low-going pulse is too small to be detected by U7B and the circuit does not function properly. --

Please replace the paragraph beginning on page 14, line 12 with the following re-written paragraph:

-- Figures 5A and 5B are schematic diagram of a third circuit (embodiment 3) according to the invention. Any "phantom" triggers caused by jitter in the phase-locked-loop circuit can be eliminated by replacing the PLL with two asynchronous crystal controlled oscillators. The problem with the PLL, as with any PLL, is slight jitter in the frequencies. A processor can easily correct the problem by taking many samples and averaging the results, especially after eliminating results that are more than a standard deviation away from the normal. But another method is used in this circuit, where two separate crystals are used. --

Please replace the paragraph beginning on page 14, line 22 with the following re-written paragraph:

-- Figures 6A and 6B are schematic diagram of a fourth circuit (Embodiment 4) according to the invention. Embodiment 4 differs from the previous embodiments in that the Length Error indicator has been removed, as well as the initial divide-by-two flip-flop that squares the pulse. As a result, this circuit allows for 1 foot resolution, or 3 ns, using the same F1 and F2 frequencies as before. No length error is provided, so cables must be limited in length or the late return pulses can cause false readings. This circuit provides excellent results for cables known to be no longer than a certain maximum length. --

Please replace the paragraph beginning on page 15, line 6 wit the following re-written paragraph:

-- Figure 7 is a flow chart of a method according to the invention. The following is a detailed explanation of the two concurrent processes depicted in Figures 6A and 6B. Parenthetical references are made to the elements of the Embodiment 1 circuit (Figures 3A-3C). --

In the Drawings:

Please replace Figs. 1-7 with the attached proposed replacement Figs. 1-7. A Drawing Transmittal Letter is attached. Upon approval of the drawing corrections, formal drawings will be submitted.